Gray Scale Image Denoising Implementation by Peres Gate

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Abstract: Excision of noise from images is a crucial task in image processing this can be attained by divergent approaches. Numerous techniques are available to implement this process. Foremost objective of this project is excision of noise in a reversible manner. Reversible logic is concentrated here as there are many benefits of using this. When we go for a reversible approach the power consumed by gates used is less comparatively. Size of reversible gates is also less so the circuit can be smaller and simple which results in reduction of the transistor count as well as its size. In this approach we have used a particular gate that is PERES gate with 4X4 and 5X5 implementation window with an image size of 1020X1024. The results got and implementation is done using Xilinx platform and a hardware implementation is carried out using a Saturn Spartan 6 Board. We have arrived on different results were we monitor the Gate Count (GC), Garbage Outputs (GO), Ancilla Inputs (AI) and Quantum Cost (QC). The specification mentioned should be as less as possible in order to get accurate results.

Keywords: Reversible circuits, Image denoising, RGB to Gray, Peres Gate, FPGA, Reversible Logic Implementation.

1. Introduction

Removal of unwanted information or noise from the transmitted image in multimedia systems is the challenge that we are facing nowadays, by removing the noise analyzing and processing of images becomes easier which is further attained by reclaiming of fine details and magnification of the image. Designing of power saving and cost effective devices with smaller size are most desirable. Researchers are concentrating mostly on devices which serve the need of power saving, compact size and also cost effectiveness. In Traditional systems the output generated cannot be reversed as the input bits are lost during generation of output bits, this results in loss which will further result in expansion of energy dissipation in the system. According to the studies which was conducted by Bennett which gave a clear idea that when the circuits were implemented by using reversible manner the energy loss of the circuit could be suppressed to zero.

The objective of this design is realization of a special type gate which is Peres gate one form of a reversible gate for refining of image present in form of gray scale. The size of window chosen for this approach is 4X4 and 5X5. In this a RGB format of image is being converted to gray scale image before the process of filtering. The approach for this is verified using FPGA SPARTAN 6 unit. Different parameters are analyzed from which we arrive at suitable results some of the parameters are AI, GC, QC and GO.

The work is organized as Section II gives the process flow of image denoising module. Section III has information about the logic used in this project. Section IV gives idea about the Denoising module for Image.Section V has topic covered on Simulation and Hardware implementation. Section VI gives the result obtained. Conclusion is provided in section VII.

2. Process Flow of Image Denoising Module

The proposed work in this paper helps in realization of a module which helps in deblurring or resampling of an image which uses a technology of reversible logic realized using Peres gate. The basic representation in terms of blocks about the denoising element is exhibited in figure 1. In this approach pixel's are fed using Pixel In which is followed by a image buffer, buffered image is processed using a 4X4 or 5X5 filtering unit finally there is a image denoise unit and Pixel Out from where we get the resultant denoised image. The denoised image got is taken in form of a relating hardware which is then viewed through the respective hardware tools required by the circuit.

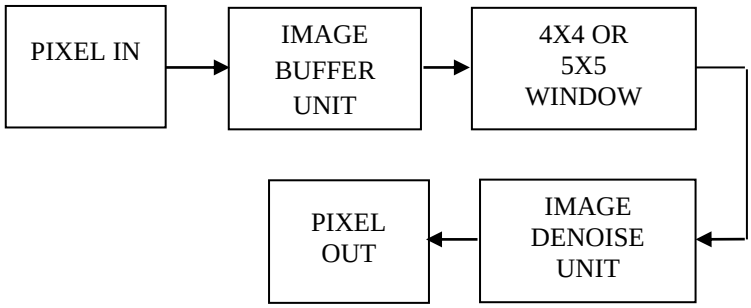

Figure 1: Image Denoising Module

2.1 Color to Gray Scale

Firstly we need to convert the image in color mode to grayscale this process is done using a MATLAB software which uses a technique of lightness. The gray value is calculated by taking the average between the lowest and highest notable color which is designated for it.

2.2 Filtering for Noise Removal

Image filtering is the process of reducing the variation of magnitude between neighboring pixels present in an image which is of 1024X1024 pixels. Noise effect in the image can be reduced mainly by regularizing the image. A unit of Mean filter is considered here which mainly has a spatial filter which is made of sliding window and available in various sizes such as 4x4, 5X5 and nXn, n is the value of number of pixels which is present in each row for the selected window.

2.3 Logic used

Reversible logic is used for the purpose of filtering. Main agenda behind using a reversible logic is the circuit dissipate zero heat and as this circuit operates in backward fashion which allows for the reproduction of inputs from the output. Advantage of using reversible logic is the power consumption is less and the chip size can also be reduced at a greater extent.

3. Reversible Logic

A principal requirement for a reversible circuit to operate is that the output and input count should be same. Some of the gates that are used commonly for this purpose are Feynman, Fredkin, Toffoli, and Peres gates which are reversible in nature. Reversible circuit must be capable of achieving logical and physical reversibility. Any circuit can be termed as reversible if input can be detected with an accuracy of 100% and not exceeding $KTln_2J$, by the grasp of output value. Logical reversibility can be attained by the method of mapping the input and output by a unique approach.

Key points that should be taken care of when we are designing a reversible circuit is

1. Input and output count must be identical.

2. For the purpose of maintaining reversibility we need to add some garbage outputs and some ancilla inputs.
3. Fan-outs and feedback paths are impermissible

Measure of effectiveness is done using different specifications available like

Ancilla Input(AI)	-	Extra inputs added to make circuit reversible.
Gate Count(GC)	-	Number of reversible gates in the circuit.
Quantum cost (QC)	-	The fundamental quantum gates needed to realize a function.
Garbage Output (GO)	-	Extra outputs added to make circuit reversible

A circuit which has least number of ancilla inputs, garbage outputs and quantum cost these circuits is much preferred in advanced and development related systems.

3.1 Peres Gate

Gate formed by 3 inputs and 3 outputs is Peres gate generally termed as (3X3) it is as shown in fig 2, quantum realization of reversible gate that is Peres gate which is used in this case is as shown in figure 3.Mapping of this gate is in terms of inputs M, N, O to the output forms as X=M, Y=M⊕N, Z=M.N⊕O. Quantum cost of the Peres gate realized is 4 as it requires 2 controlled V+ gates, one controlled V gate and one CNOT gate. In comparison with other reversible gates the Peres gate has the minimum quantum cost.

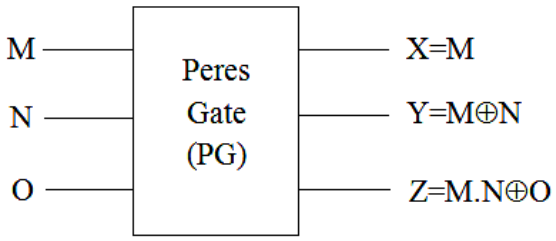

Figure 2: Image Denoising Module

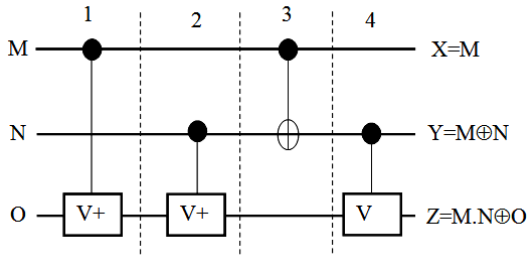

Figure 3: Image Denoising Module

4. Denoising Module for Image

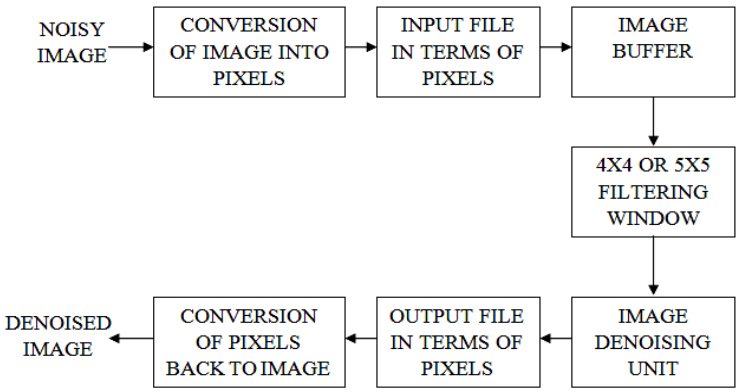

Figure 4: Block diagrammatic representation of Implementation Process

Implementation module of denoising is arrived out in different blocks as in figure 4. We are using a bottom up design approach were we are designing the basic part in first mode then we are linking it to the higher one then next step until the final module of approach is reached. As the process is divided into different blocks first we start with the conversion of the color image into grayscale this is usually done with a help of a MATLAB software were a colored image is fed to the unit and an output of grayscale image is received. Image needs to be converted into grayscale because the algorithm which we use for the purpose of processing is simple comparatively. When we are processing a RGB image sometimes the information may not be necessary for the purpose of processing so we may skip this which in turn reduces the complexity of algorithm the time consumed can be lowered and with all this the speed of the processing can also be increased at a greater extent. Compared to color images the noise reduction can be easily and accurately done in case of Grayscale images then color images.

Information got from grayscale image needs to be converted into suitable pixels of data where the processing operation is carried out. For the purpose of processing again we are adding noise component to the image via MATLAB tool. Noisy image is converted into pixels of data this now acts as an input for the Xilinx platform. We mainly have two parts in that image buffer to store the pixels of data and to process it in step by step manner the image which we have selected is of the size 1024X1024 so at a time all the pixels cannot be processed in a single click we need to process them in parts so we require image buffer for this.

Filtering window which we have chosen is 4X4 and 5X5 in both the window we have started from the basic logic of Peres gate then we go to the full adders next is the ripple carry adder and finally we are combining all this together and we get a complete processing unit. In this the noisy image is processed and final output got from this is again a file which has data in the form of pixels we cannot directly read the data and check the result but it needs again to be fed to MATLAB where the Pixel data got needs to be converted back to a image form. Final image got has reduced the noise at a greater extent and we can use it for further purpose.

Image denoise unit is designed using bottom up approach is as shown in figure 6, here we are starting the design with a reversible Peres gate which has a low quantum cost. Using this Peres gate we have designed a full adder unit these units are combined and we design a Ripple Carry Adder. For 5X5 approach we have 25 inputs these are fed to the unit via twelve 8-bit adders and a remaining one bit is directly fed to an 11-bit adder. Output of 8-bit adder is fed to six 9-bit adders which are then followed by three 10-bit adders. Output got from 10- bit adder is given to two 11-bit adders finally the unit is connected to a single 12-bit adder at last output is drawn and we are getting a denoised image.

4.1 Full adder Peres Gate

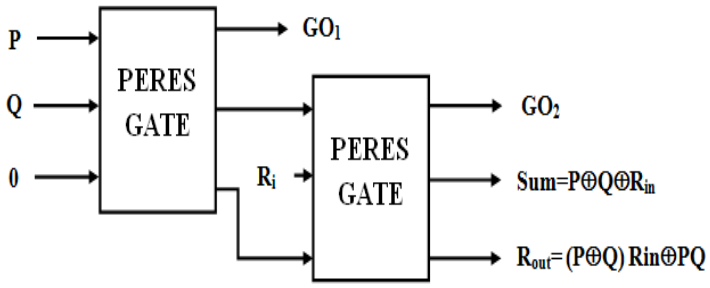

Figure 5: Reversible Peres gate Full Adder

Designing of a full adder using a reversible logic requires two Peres gate in which it has two garbage outputs and one constant input gate used is of order 3X3 it has 3 inputs and 3 outputs. Full adder is as sown in figure 5 GO1 and GO2 indicate the garbage outputs the expression for full adder is given by Sum=P⊕Q⊕Rin and Rout=(P⊕Q)Rin⊕PQ here P, Q are inputs and Rin is Carry in and Rout is Carry out. We have constructed full adder because it acts as a fundamental building block in different computational units. In this design after the reversible Peres gate Full adder occupies the next higher step in the process of design approach.

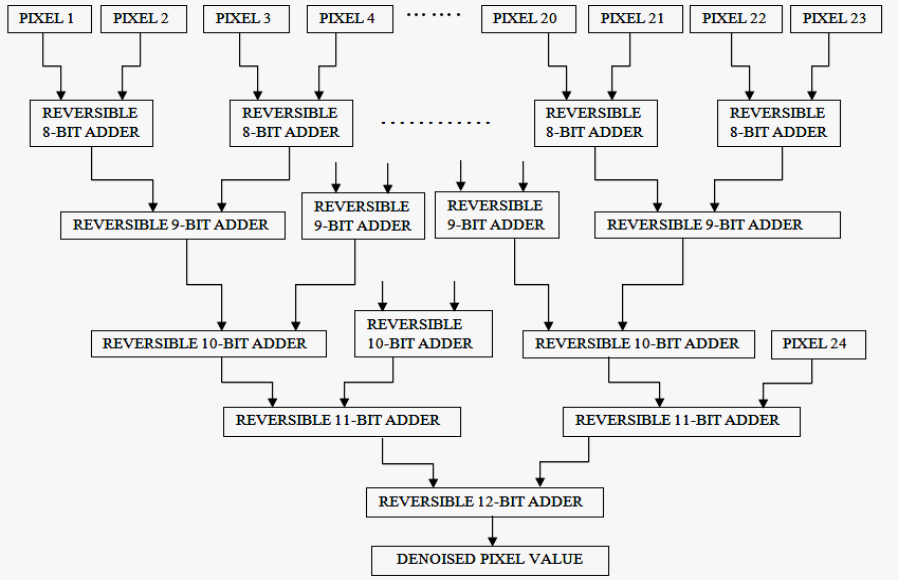

Figure 6: Reversible Mean Filtering Unit with window size of 5X5

5. Implementation Methodology

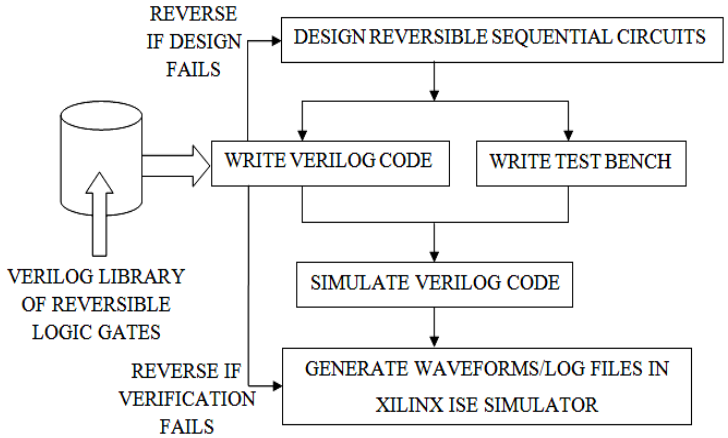

Figure 7: Representation of Simulation Process

The simulation process was realized using Xilinx ISE platform were the library files of required reversible logic were added then the design approach was done by bottom up fashion where a reversible gate basic element was written and followed by a set of other full adders and ripple carry adders were used. We have used Xilinx ISE simulator for the process of writing the verilog code and test benches required. Resultant waveforms generated were obtained by the same platform. The complete simulation process is shown in figure 7.

It is mainly divided into 3 parts

1. Respective file generation for conversion to gray scale.
2. Process of Denoising using Peres gate to filter using 4X4 and 5X5 algorithms.
3. Display the file generated with the help of VGA.

In this process the original color image which is of size 1024X1024 needs to be converted into grayscale as filtering process for grayscale images can be done in a easy manner and the results of the filtering achieved is much more accurate.

In this approach pixel value of image got from MATLAB is fed to the Xilinx software here we are carrying out the process of filtering by reversible logic selecting a Peres gate for realization of window size 4X4 and 5X5 using a Bottom up approach for the purpose of designing. The output file which contains values of pixels again needs to be sent to MATLAB for display purpose.

In this part of implementation the resultant data got from the approach of Xilinx platform is fed to MATLABin which we convert the pixel data back into a suitable image format which is the denoised image final output.

5.1 Hardware Part

Hardware part implementation unit mainly requires a Saturn Spartan 6 hardware module, PmodVGA, VGA cable and a display unit (monitor).The verilog file generated for a hardware part which is in bin format that needs to be dumped into the Xilinx board with the help of a SATURN driver module. There is presence of EPROM to store the bin file generated this will load the data to Xilinx IC in order to process and the image is displayed on to VGA unit with the help of another interface which converts the data of RGB got into suitable VGA format there is a presence of h_sync and v_sync to display the data across VGA.

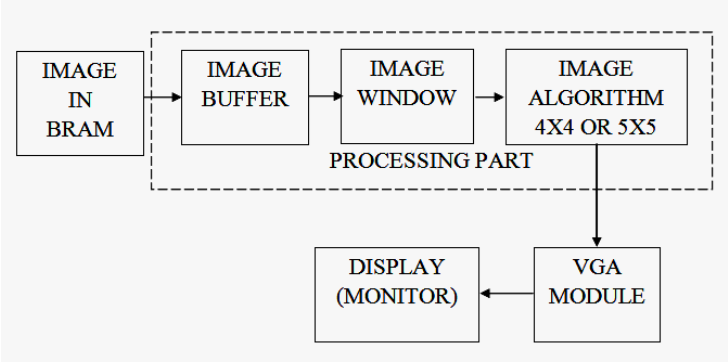

Figure 8: Hardware implementation of Image output

8. Result

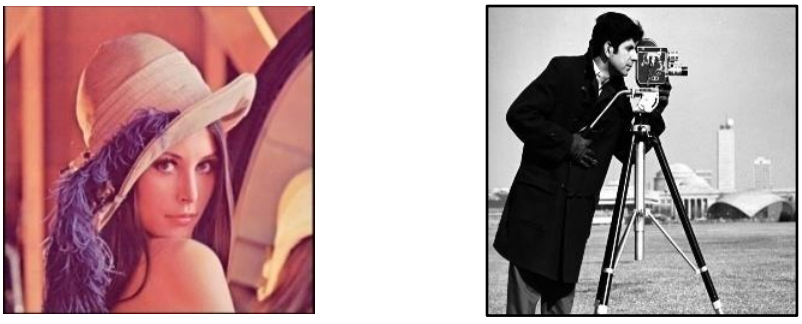

Figure 8: Original Image for Denoising Module

Figure 9: Gray Scale Image with Noise

Figure 10: Output after 5X5 Filtering(Denoised Image)

Efficiency of reversible gates is verified by different parameters like ancilla input, gate count, quantum cost and garbage outputs table 9.1 illustrates clearly about the parameter value obtained of adders and finally we get value of complete denoising unit in which we have considered 4X4 and 5X5 window.

Table 9.1 Reversible parameters obtained for complete denoising unit.

Design Block	**AI**	**GC**	**QC**	**GO**
8-Bit Adder	0	16	64	24
9-Bit Adder	0	18	72	27
10-Bit Adder	0	20	80	30
11-Bit adder	0	22	88	33
12-Bit Adder	0	24	96	36
Complete Image Denoising Unit				
4X4 window size	0	262	1048	393
5X5 window size	0	428	1712	637

Quality of the image obtained is verified by the measure of Peak signal to noise ratio were a higher value of PSNR will indicate the quality of the regenerated or the compressed image is good. Mean square error is interlinked with PSNR the MSE will be present in denominator as low the value of MSE the higher will be the value of PSNR. Detailed output obtained for the images is as illustrated in table 9.2.

Table 9.2 Resultant values obtained for PSNR and MSE

Image	**Window Size**	**PSNR**	**MSE**

Lena	4X4	26.5638	173.4971
Lena	5X5	25.8553	168.8695
Cameraman	4X4	26.7563	171.6908
Cameraman	5X5	25.9213	166.3238

8. Conclusion

In this project we have implemented an Image denoising unit which works on reversible logic approach. Image of size 1024X1024 color image is taken for purpose of realization firstly converted to grayscale for the purpose of processing and is then implemented using a 4X4 and 5X5 image window. Processing part is done using a particular gate called PERES gate as it has low Quantum cost. The whole design is built on bottom up approach. Result of Simulation part is observed using Xilinx ISE modulator and hardware part implementation is done using Saturn Spartan 6 board and result obtained is viewed on VGA display.

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