Voltage over Scaling-Based Dadda Multipliers for Energy-Efficient Accuracy Design Exploration

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Abstract: An X-DADDA multiplier that is both energy-efficient and accurate is the subject of this article. Voltage scaling and approximate width setting approximation controls boost the multiplier's energy usage and dependability while extending its lifespan. The latter can only be utilised before and after design, unlike the former, which can be modified at any time. A certain degree of precision is required in order to calculate the partial product columns and the over scaled voltage in order to maximise energy. Columns with lower bit significances and more switching activity are commonly used to keep the inaccuracy within a reasonable range. Level shifters are used rarely in this design due of their low cost. Every column following the first one is connected to each other. If you want more efficiency from your multiplier, you should reduce the output from it to only four bits. 15-nm FinFET technology is used to investigate the X-Dadda structure's efficiency. Approximation based on the typical relative error distance of 0.11 can save up to 43% of the power consumed in a home. Bias temperature instability (BTI) is reduced by up to 9.9 percent in this case compared to the precise mode when the delay degradation is 50%. The X-accuracy Dadda's also investigate the influence of process adjustments. Finally, the X-Dadda multiplier is put to the test in neural networks for image categorization and processing.

Index Terms:- An energy-efficient multiplier, a customizable multiplier (AxC), voltage scaling (VOS).

1. INTRODUCTION

For embedded CPUs, power consumption is critical. It's because some programmes have heavy workloads and must operate within a specific power budget. A work's energy requirements should be maintained as low as possible in order to accomplish this goal. Computer systems can be made more energy efficient by using approximation computing (AxC). This paradigm can be employed if the impact of computation errors on output quality degradation is tolerable. At many levels of

abstraction in design, AxC can be used effectively. One technique for hardware approximation is to lower the circuit supply voltage below its typical error-free value. It's a process called voltage scaling (VOS).

With VOS, the AxC paradigm may be realised while simultaneously enhancing energy efficiency, longevity, and reliability. This is especially important in the case of current-generation technologies that have been extensively scaled up[1]. As a result, it has become increasingly challenging to design digital systems that meet reliability and life expectancy standards. The VOS approach has an additional benefit of precise configurability because it may modify the VOS level while running.

The process of removing or simplifying parts of a circuit's gates in order to make it more energy efficient is known as "circuit pruning." Based on these ideas, a number of approximation multipliers have been proposed in the literature. Numerous research have been carried out to examine the properties of the numerous different approximate multipliers as a result of the large amount of data available[2].

The X-Dadda multiplier is proposed and examined in this study (VOS-based Dadda multiplier). Two different topologies are compared based on differences in estimated column counts and VOS voltage levels. Take a look at these highlights from the essay[3].

- An approximation is created and analysed using the VOS method. The Dadda multiplier's structure
- An approximation multiplier with little overhead that can be fine-tuned at runtime is being proposed.
- An investigation into the accuracy and energy consumption of the X-Dadda multiplier is being carried out by applying various approximate bit widths with or without truncation at six VOS voltage levels (the higher number of VOS voltage levels provide a higher accuracy granularity for the X-Dadda multiplier.) The X-Dadda multiplier hardware is being improved by using the VOS method.
- The influence of process variation (PV) on the X-Dadda multiplier output error for various VOS voltage levels is currently being researched.

2. RELATED WORK

8X8 DADDA MULTIPLIER

In order to determine the impact of implementing the suggested blowers, an 8x8-fold unsigned Dadda tree multiplier is used. For each midway item, the recommended multiplier is applied in the preliminary portion and at the entrances. There are fewer incomplete devices in the CSA tree because it uses blowers proposed in the field. Using an exact CPA[4], the final double end result

can be calculated. A given multiplier's hardware needs to be scaled back to accommodate n=eight. Half-adders, full-adders, and four-2 blowers are utilised in the reduction phase of this figure; each object bit is handled by a spot. Half-and-full adders are used to divide the midway items into four columns, while eight blowers are used in the first setup[5]. The final two columns of midway items are treated with a half-viper, a full adder, and 10 blowers in the second or final step.

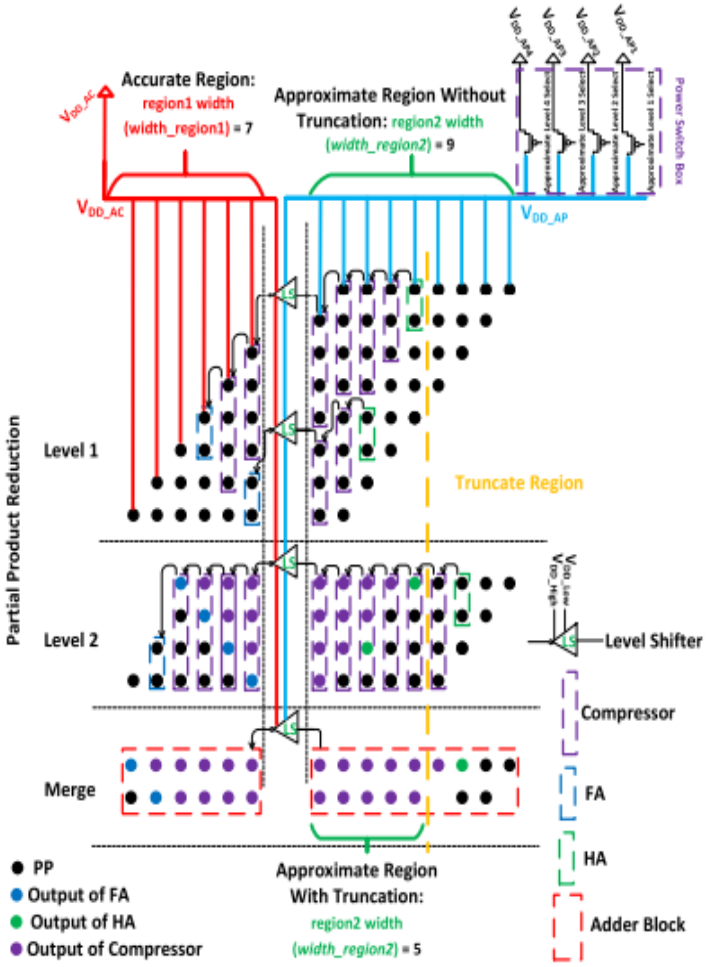

Figure1: 8x8 Dadda Multiplier

When the electrons' vitality matches one of the allowed levels of vitality in the well, the vitality is considered to be "in harmony." The pinnacle current (also known as the pinnacle voltage, or Vp) flows through a device when its highest possible current is operating at this enormous voltage (Ip). If current flow through the device is reduced as voltage rises, so too does burrowing. This continues until the voltage reaches what is termed as the "valley voltage" (Vv). The valley current is the name given to the current flowing at this voltage (Iv)[6]. Circuits with high speed and small size can benefit from the usage of negative differential opposition. For diodes that do not lead, a voltage of

Vp indicates the maximum conductance, while one of Vl indicates the lowest conductance. Figure 3 illustrates this relationship between voltage and conductance (Vv). You can tell a lot about an RTD's capabilities by examining the sharpness of its voltage-current plots. Based on this ratio, an educated guess can be made.

VOLTAGE SCALING

Dynamic power consumption is inversely related to the supply voltage, therefore even a minor increase or reduction can have quadratic effects[7]. Parallelism, pipelining, threshold voltage reduction, and Multi-Vdd must be implemented in order to compensate for the performance losses caused by reducing the supply voltage. In this part, we'll look at some of the most common methods for compensating for the speed disadvantage that comes with voltage scaling.

Multi Voltage Design

Different Vdd voltages can be injected into the system in order to protect critical circuit components while minimising areas where speed loss is acceptable. "Multi-voltage design" is a technique for reducing a system's overall power consumption by using multiple supply rails to supply different voltage levels to different sub-circuits[8].

Variable voltage levels can be applied to a circuit or a series of subcircuits in two ways:

Static Voltage Scaling:

In order for designs to perform at different levels, a variety of diverse blocks are required. The higher the voltage, the better the throughput, whereas slower sub-systems can use a lower voltage to save electricity.

Adaptive Voltage Scaling:

System or discrete voltage zones can be dynamically applied with different voltages based on the workload or performance requirements.

Multi-voltage designs necessitate several power rails, which not only introduces new design issues due to the need to connect blocks in various supply voltage regions, but they also necessitate circuit characterization at various voltage levels[9]. A some of the challenges we face:

- Level shifters were required to connect blocks from different voltage ranges.
- All voltage partitions should be subjected to a worst-case scenario characterization and timing analysis to ensure that time requirements are met.
- Many power networks coexist on a single chip, resulting in a rise in the complexity of the floor layouts.
- Procedures for powering on and shutting down the system must be defined in order to avoid a stalemate and a system failure.

Parallelism

Although it is feasible to minimise the overall energy usage by parallelizing specific elements of a DSP process, this involves the addition of area penalties. Allowing lower supply voltages and the adoption of more power-efficient, slower cells has resulted in an increase in processing time as a result of parallel-working blocks.

The ability to run at a certain clock frequency (fclk) is required in some systems. Instead of many adders, the basic version uses a single one. System parallelism allows for the creation of two sluggish adders to do the same tasks in parallel, albeit at the cost of a bigger footprint. In this case, we assume that the dynamic power consumption of the original single adder design at frequency $f_{clk} = P_{ref.}$

$$P_{ref} = f_{clk} \cdot C_{ref} \cdot V_{dd}^2$$

The same throughput may be achieved by operating two adders in parallel at half the original clock frequency $f_{clk}/2$, but this would necessitate replicating the original adder structure and coordinating the parallel operations. Two adders can be powered with an approximation of their combined power using an equation or other reasoning.

$$P_{parallel} = (f_{clk}/2) \cdot (2.4 \cdot C_{ref}) \cdot V_{dd}^2 = 1.2 \cdot P_{ref}$$

Operating frequency can be decreased to f/2 and lower power consumption cells like highVT can be used to reduce the supply voltage's operating voltage[10]. Clock speed reductions can be used to estimate power by assuming that the original supply voltage can be scaled by 0.8.

$$P_{parallel-VS} = \frac{f}{2} \cdot 2.4 \cdot C_{ref} \cdot (0.8 \cdot V_{dd})^2 \approx 0.77 \cdot P_{ref}$$

The lower dynamic power consumption at the expense of an increased silicon area required to implement the device is offset by a 20 percent overhead for circuitry that controls parallel processes, according to the statistics for power usage.

Pipelining

It is also possible to use pipelining to do a large number of tasks or components of an activity simultaneously. Extra registers can be inserted between logic stages using this method[11], allowing complex operations to be separated into smaller pieces that can be performed independently and with fewer time constraints.

Although it boosts overall system performance by increasing the number of registers and reducing latency, pipelining is more energy- and space-intensive than either method alone. Due to the lack of circuit replication, pipelining has a smaller area overhead than parallelism.

VOLTAGE OVER-SCALING (VOS)

When designing and implementing energy-efficient very large scale integrated circuits (VLSI), a technique called voltage scaling can be applied. It is possible to reduce the primary dynamic power consumption by a factor of K2 by raising the supply voltage. Integration was made possible by the growth of CMOS technology[12]. As a result of these changes, there was an exponential growth in the number of design concerns. Strict design limitations can be imposed as a result of changes in a circuit's critical path, which can lead to conservative designs with excessive power consumption.

Due to lower system performance, gate responsiveness in design decreases when supply voltage is decreased below the minimal threshold required for cautious Vddcrit approach. In fault-tolerant technique assessments, the Alpha-power model is the most commonly used representation of decreased transistor performance. This model's definition of the circuit delay-supply voltage relationship looks like this.

$$\tau_d = \frac{C_L V_{dd}}{\beta(V_{dd} - V_t)^\alpha}$$

The capacitance of the load, the transconductance of the gate, the threshold voltage, and the saturation index are all represented by the letters CL, Gt, Vt, and Vs, respectively. Detailed information about the Alpha-power delay model can be found in Appendix C. VOS throws off the timing of the circuit when it activates the circuit's important routes[13]. A trade-off between energy savings from supply scaling and corrective loads can be achieved using techniques that allow the use of VOS on arithmetic circuits, due to the wide variation in average and worst-case circuit delays.

It had previously been studied as a method of extending the cautious usage of DVS and increasing energy efficiency by using error-resiliency or fault tolerance.

Traditionally, the worst-case safety margins have been limited by a design's failure. Circuits with virtually no worst-case safety margins can be built by actively adjusting the circuit operating point while dynamically monitoring the error rate[14]. System performance and energy efficiency can be greatly enhanced as a result, compared to traditional techniques.

EFFICACY OF ACM IN GAUSSIAN FILTER

The proposed multiplier is demonstrated in practice using a Gaussian smoothing filter (GSF). Gaussian smoothing is achieved via convolution of the input picture sub-matrix with the Gaussian kernel

$$\frac{1}{2^8}\begin{bmatrix} 1 & 3 & 6 & 3 & 1 \\ 3 & 15 & 25 & 15 & 3 \\ 6 & 25 & 41 & 25 & 6 \\ 3 & 15 & 25 & 15 & 3 \\ 1 & 3 & 6 & 3 & 1 \end{bmatrix} * \begin{bmatrix} P_{11} & P_{12} & P_{13} & P_{14} & P_{15} \\ P_{21} & P_{22} & P_{23} & P_{24} & P_{25} \\ P_{31} & P_{32} & P_{33} & P_{34} & P_{35} \\ P_{41} & P_{42} & P_{43} & P_{44} & P_{45} \\ P_{51} & P_{52} & P_{53} & P_{54} & P_{55} \end{bmatrix}$$

The 8-bit approximate multipliers introduced in the convolution are used for other operations, such as addition and division. Verilog netlists with variable multipliers were developed for all of the designs using Synopsys Design Compiler and a 90nm PDK. ACM-embedded filters use 53.8% less power than filters embedded with suitable multipliers (46.02%), truncated multipliers (46.02%), or UDM multipliers (14.48%), according to post-synthesis simulation data. There is a significant reduction in filter area and delay with this decrease in power. Finally, compared to UDM and Truncate multiplier solutions, the suggested ACM saves 21.2% and 39.9%, respectively. A high-quality energy tradeoff is provided by the suggested multiplier in applications such as the discrete cosine transform (DCT), edge detection, and other image-enhancing techniques, as well as the GSF. Models of these filters and benchmark images like Lena, Mandrill, and others are used to derive image quality metrics like PSNR and SSIM. According to the Table, the proposed multiplier has better quality metrics than the current multiplier. When utilizing an ACM integrated filter, PSNR is 7.71dB better than ETM and 1.28dB better than Truncate multipliers. More importantly, the ACM embedded filter has a substantially lower degree of error, which implies that the recommended multiplier for image filtering applications can result in significantly increased energy efficiency with less image quality loss. While the Truncate/ETM embedded filter[15] causes noise in its output photos, ACM's image quality reduction is modest and can be tolerated by the human eye.

Parameter	Accurate	Truncate	ETM	UDM	ACM
PSNR (dB)	26.75	24.082	17.61	26.74	25.32
SSIM	0.8648	0.8622	0.7882	0.8641	0.860
FSIM	0.9498	0.9478	0.9137	0.9486	0.948
Area(μm^2)	166040	98636	95315	135339	130616
Power (mW)	23.38	20.01	6.64	12.63	10.8
Delay (nS)	79.67	62.34	43.29	75.96	69.36
PDP (pJ)	1862.7	1247.4	287.4	959.4	749.0

Table1: Design and quality metrics for various 8-bit multipliers

3. DESIGN AND ANALYSIS

DADDA MULTIPLIER DESIGN

Addition and multiplication are the most typical operations in a multiplier circuit. In mathematics, we call these operations "arithmetic." The approximation computation is handled by a complete adder circuit in these devices. Several different methods are used to assess the relative merits of various adders. It is possible to build approximation and probabilistic adders using the various applications. It is possible to use these adders in a wide range of computational tasks. Each circuit's interferences and errors can be calculated using the output and the rectified input. To measure the arithmetic error between an incorrect output and the correct output of a circuit, the term "error distance" is used (ED). For these distances, the average effect of various inputs and the normalization of multibit adders are taken into consideration. The multiplexer's size and robustness both play a role in determining the NED[16]. Precision versus power has also been evaluated objectively. When it comes to guess multipliers, though, there has been less focus. Solely approximating adders while planning for a hypothetical multiplier can be extremely wasteful in terms of accuracy, gear complexity, and other implementation concerns. A few simple multipliers were incorporated in the works of the authors. Truncated growth is used in the vast majority of these structures, in which only the most insignificant parts of the finished devices are monitored on a regular basis. A cluster multiplier may overlook some of the tiniest bits in the center gadgets for neural technique purposes (and on this method expelling a few adders within the cluster)[17].

Using a comfort regular and a truncated multiplier is recommended. One half of each half-way object is brought together for a nn multiplier, and the other half is reduced in size. As soon as this is done, the n+ok bit's impact is reduced to n bits only. We now need to look for difficulties, such as truncating the previously accepted least significant bits or changing the result to n bits, which can result in errors like those indicated above. As close as possible to the evaluated estimation of all these faults is chosen in order to minimize error disposal. Finally, the multiplier's structure has received far less attention. Because of the waste of precision, apparatus complexity, and other execution metrics that this could create, it is not practicable to use difficult adders directly while generating an inexact multiplier. There were a slew of different possible multipliers mentioned in the text. It is common practice to use the most central parts of the half-way devices as a starting point for building the rest of the structure. Because only a few of the least important bits of the fractional elements matter in an uncertain cluster, an uncertain cluster multiplier is employed for neural approach reasons (and for this reason expelling just a few adders within the cluster). It has been proposed that a multiplier with a shorter length and an uniform relief be utilized.

The n+k biggest segments of all fractional gadgets can be computed using this structure while also truncating their opposing n-okay segments for a nn multiplier's n-ok segments. To reduce the n+k bit results to the n bit size, the n+k bit outcomes are lowered. Reduction and correction errors are reported in the next phase. Reduction mistakes and adjustment errors are included in this (e.g., reducing the results to the last K bits). So that errors can be separated more easily, we choose the modification constant (n+k bits) to match our predicted estimates as closely as possible.

4. SIMULATION RESULTS

A hardware description language, HDL (Verilog HDL) (HDL). The Hardware Description Language (HDL) programming language can be used to describe a laptop or computer system (HDL). A complex framework can be depicted using only a few dimensions. In the swap stage of an IC, an HDL, for example, can paint the wiring, resistors, and transistors. To mark the beginning of a complex structure, which incorporates practical entryways and flip tumbles, it might be used. Decomposed modules were found to have Verilog activity yields. The following are some of the end results:

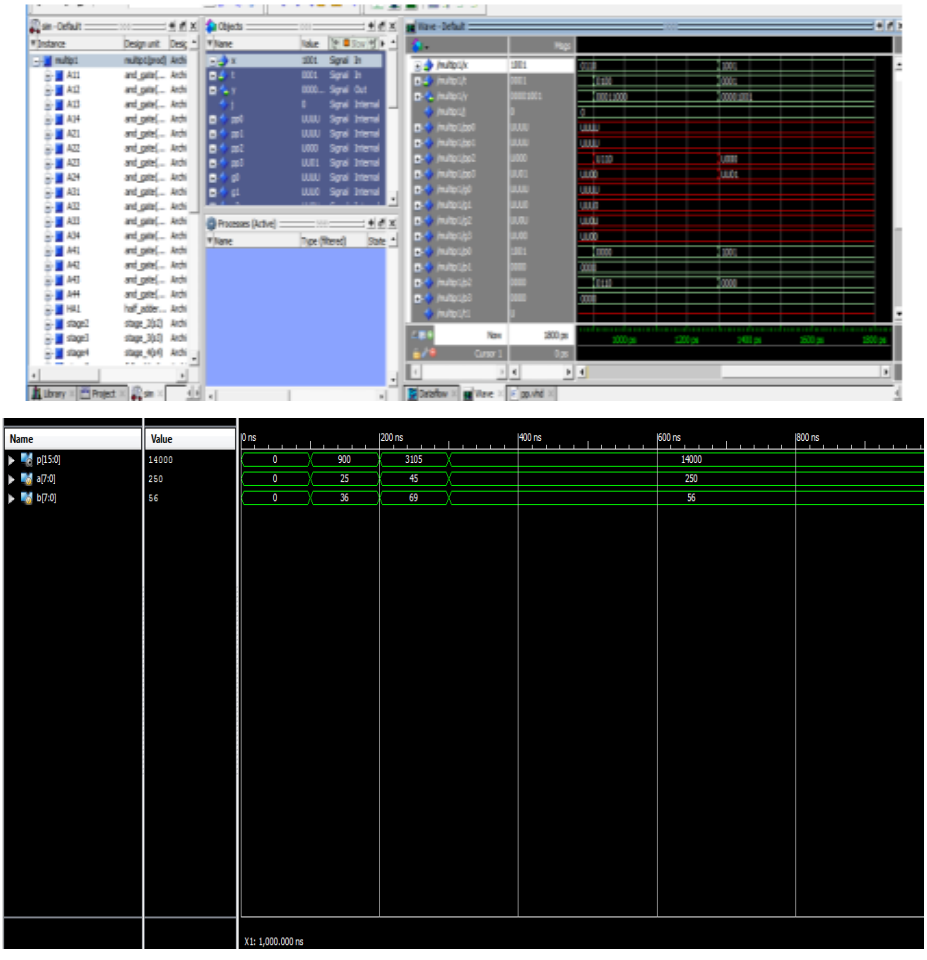

Figure2: Exact compressor Verilog output waveform.

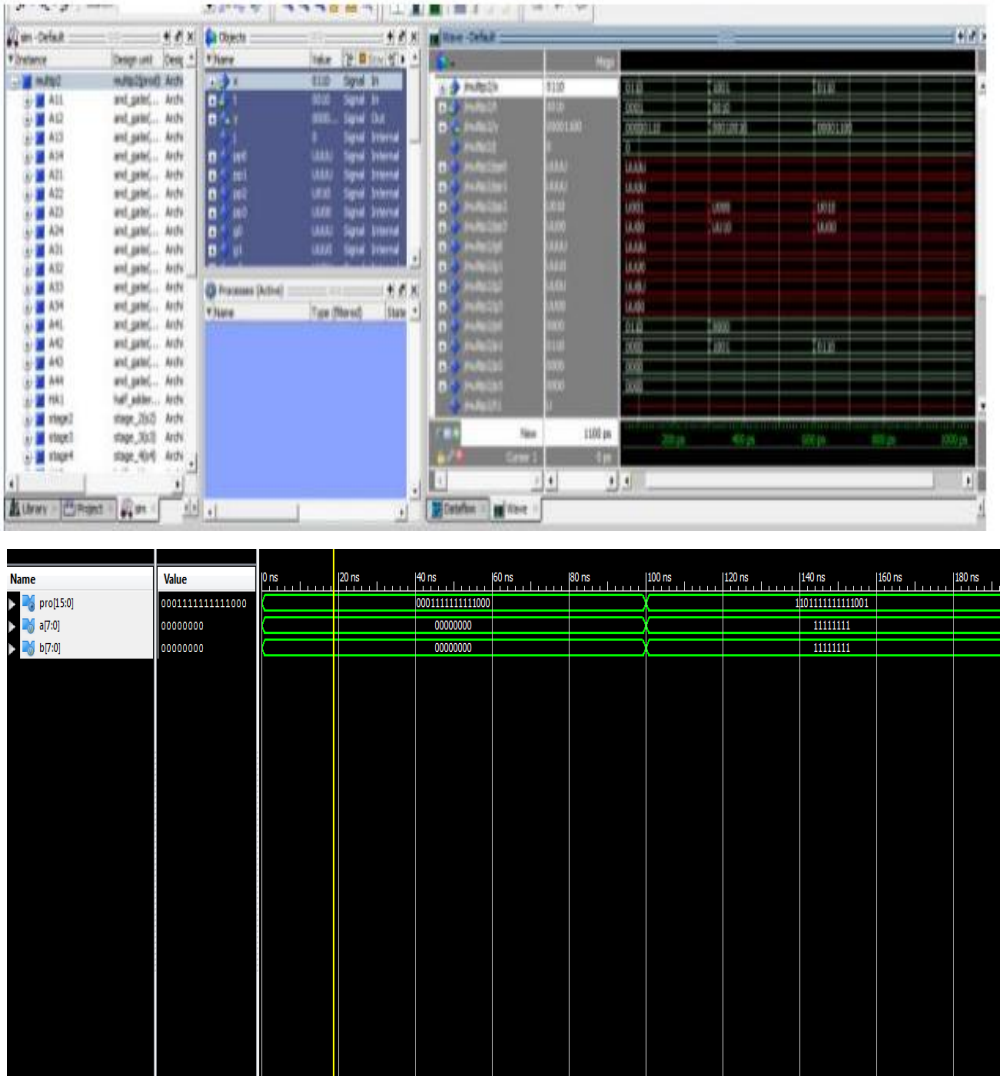

Figure3: Approximate compressor design 1 Verilog output waveform

```
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 11.582ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 91 / 8
---------------------------------------------------------
Delay:               11.582ns (Levels of Logic = 8)
  Source:            t<4> (PAD)
  Destination:       y<7> (PAD)
```

Figure Exact compressor Verilog output parameters

```
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 7.796ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 40 / 8
---------------------------------------------------------
Delay:               7.796ns (Levels of Logic = 4)
  Source:            x<2> (PAD)
  Destination:       y<2> (PAD)
```

Figure. Approximate compressor design 1 Verilog output parameters

The illustration depicts a MATLAB image.

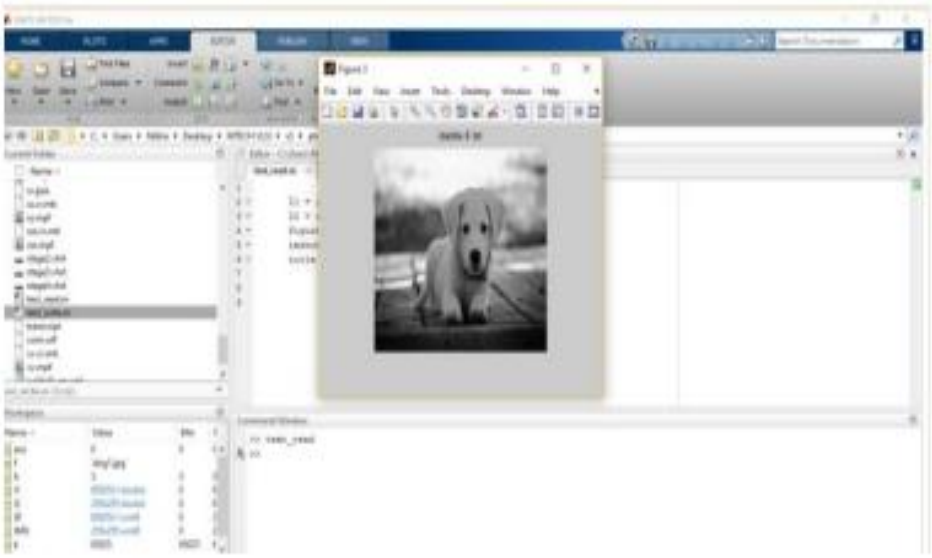

Figure4: output of dadda multiplier in image

5. IMPLEMENTATION OF PROPOSED COMPRESSOR IN SYSTOLIC ARRAY BASED DIGITAL FILTER

Compressor performance can be evaluated using a systolic array-based digital filter shown in this figure. Carry look ahead adders and Wallace tree multipliers are among the cutting-edge components in this division. An estimate of how much area, latency, and power dissipation a digital filter will consume is presented in the following table. At 180 nm and 90 nm, the digital filter and compressor reduce PDP by at least 8.67% and 6.98%, respectively, compared to other cutting-edge technologies. These graphs illustrate PDP plots for digital filter compressors with 180 nm and 90 nm technology, respectively[18].

A comparison of suggested and other cutting-edge compressor designs with the area, latency, and power consumption of digital filters.

Performance Metrics Compressors		Area (μm^2)	Delay (ns)	Power (μW)	PDP (μW-ns)
180 nm	Using Conventional Compressor	13567	21.103	1.852	39.083
	Using Logic Level Optimized Compressor (Chang et al.2004)	18736	14.924	2.422	36.146
	Using High Speed Compressor (Baran et al. 2010)	19679	14.691	2.702	39.695
	Using Logical Decomposed Compressor (Pishvaie et al.2013)	18212	15.172	2.360	35.806
	Using Ultra High Speed Compressor (Aliparast et al. 2013)	19212	14.107	2.456	34.647
	Using Proposed Compressor	15530	15.573	2.032	31.644
90 nm	Using Conventional Compressor	6887	13.976	0.802	11.209
	Using Logic Level Optimized Compressor (Chang et al.2004)	9511	9.884	1.049	10.368
	Using High Speed Compressor (Baran et al.2010)	9989	9.729	1.170	11383
	Using Logical Decomposed Compressor (Pishvaie et al. 2013)	9245	10.048	1.022	10.269
	Using Ultra High Speed Compressor (Aliparast et al. 2013)	9752	9.342	1.083	10.117
	Using Proposed Compressor	7934	10.446	0.901	9.412

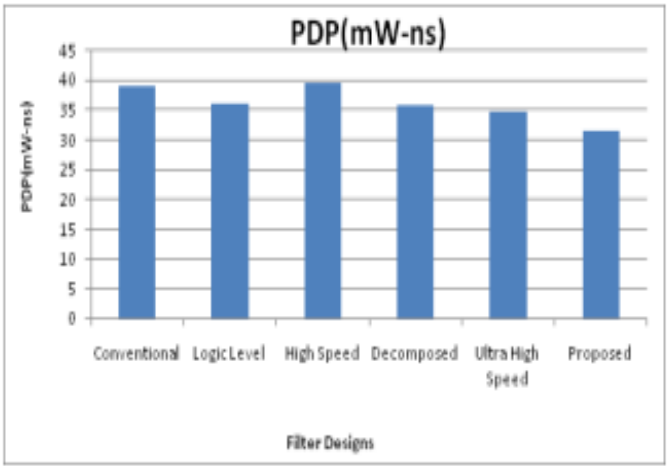

Figure 5: Proposed Compressor Design for 180nm Filter PDP Implementation Using 180nm Technology

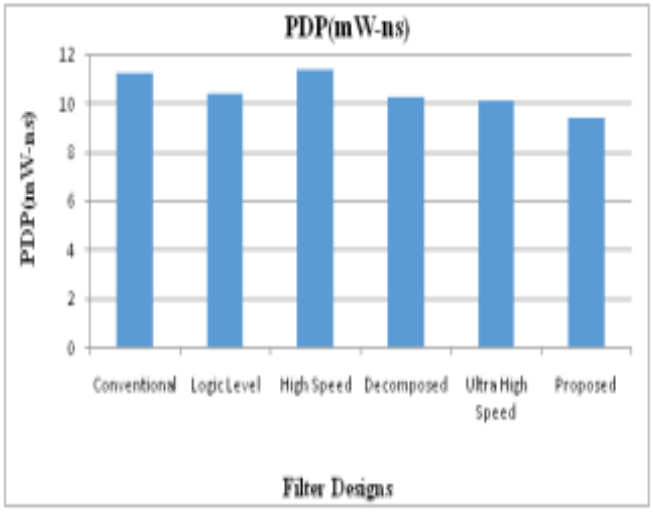

Figure: 6 The proposed compressor and current state-of-the-art designs were used to create the Digital Filter PDP for 90 nm Technology.

6. CONCLUSION

X-Dadda (VOS-based X-Dadda) is a customizable X-Dadda explained in this article. Energy consumption decreased and life expectancy improved as a result. The X-Dadda multiplier could operate in either approximate or exact mode at any time throughout system operation if the approximation part's working voltage remained constant. Accuracy, energy consumption, and lifetime of the multiplier were all assessed by looking at its approximation width and the voltage level that was applied. After cutting the part's width in half and reducing its operating voltage by half, the multiplier used 21% less energy at a cost of 0.057 MRED.

REFERENCES

[1]. Srinivas, L., & Umapathi, N. (2022, May). New realization of low area and high-performance Wallace tree multipliers using booth recoding unit. In *AIP Conference Proceedings* (Vol. 2393, No. 1, p. 020221). AIP Publishing LLC.

[2]. N. Umapathi, G. M. Krishna and L. Srinivas, "A Comprehensive Survey on Distinctive Implementations of Carry Select Adder," *2021 4th Biennial International Conference on Nascent Technologies in Engineering (ICNTE)*, 2021, pp. 1-5, doi: 10.1109/ICNTE51185.2021.9487718.

[3]. F. Nakhaee, M. Kamal, A. Afzali-Kusha, M. Pedram, S. M. Fakhraie, and H. Dorosti, “Lifetime improvement by exploiting aggressive voltage scaling during runtime of error-resilient applications,” Integration, vol. 61, pp. 29–38, Mar. 2018.

[4]. H. Afzali-Kusha, O. Akbari, M. Kamal, and M. Pedram, “Energy consumption and lifetime improvement of coarse-grained reconfigurable architectures targeting low-power error-tolerant applications,” in Proc. Great Lakes Symp. VLSI (GLSVLSI), 2018, pp. 431–434.

[5]. S. Reda and M. Shafique, Approximate Circuits—Methodologies and CAD. Cham, Switzerland: Springer, 2019.

[6]. H. Jiang et al., “Characterizing approximate adders and multipliers optimized under different design constraints,” in Proc. Great Lakes Symp. VLSI (GLSVLSI), 2019, pp. 393–398.

[7]. D. Esposito, A. G. M. Strollo, E. Napoli, D. De Caro, and N. Petra, “Approximate multipliers based on new approximate compressors,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 12, pp. 4169–4182, Dec. 2018.

[8]. J. Liang, J. Han, F. Lombardi, “New Metrics for the Reliability of Approximate and Probabilistic Adders,” IEEE Transactions on Computers,vol. 63, no. 9, pp. 1760 - 1771, 2013.

[9]. V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, K. Roy, “IMPACT: IMPrecise adders for low-power approximate computing,” Low Power Electronics and Design (ISLPED) 2011 International Symposium on. 1-3 Aug. 2011.

[10]. S. Cheemalavagu, P. Korkmaz, K.V. Palem, B.E.S. Akgul, and L.N. wChakrapani, “A probabilistic CMOS switch and its realization by exploiting noise,” in Proc. IFIP-VLSI SoC, Perth, Western Australia, Oct. 2005.

[11]. Zhu N, Goh WL, Zhang W, Yeo KS, Kong ZH (2010) Design of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing. In IEEE Transactions on Very Large Scale Integration (VLSI) Systems 18(8):1225– 1229

[12]. Kulkarni P, Gupta P, Ercegovac M (2011) Trading accuracy for power with an underdesigned multiplier architecture. In: Proceedings of the 24th international conference on VLSI design (VLSID), pp 346–351

[13]. Murali Krishna G., Karthick G., Umapathi N. (2021) Design of Dynamic Comparator for Low-Power and High-Speed Applications. In: Kumar A., Mozar S. (eds) ICCCE 2020. Lecture Notes in Electrical Engineering, vol 698. Springer, Singapore. https://doi.org/10.1007/978-981-15-7961-5_110

[14]. Zhu N, Goh WL, Wang G, Yeo KS (2010) Enhanced low-power high-speed adder for error-tolerant application. In: Proceedings of the international SoC design conference (ISOCC), pp 323–327 6. Momeni A, Han J, Montuschi P, Lombardi F (2015) Design and analysis of approximate compressors for multiplication. IEEE Trans Comput 64(4):984–994

[15]. Aliparast, P, Koozehkanani, ZD & Nazari, F 2013, "An Ultra High Speed Digital 4-2 Compressor in 65-nm CMOS", International Journal of Computer Theory and Engineering, vol. 5, no. 4, pp. 593-597.

[16]. Shams, AM & Bayoumi, MA 1997, 'A structured approach for designing low power adders', In IEEE Conference Record of the Thirty-First Asilomar Conference on Signals, Systems & Computers, vol. 1, pp. 757-761

[17]. Huang, SC, Wang, HM & Chen, WY 2012, 'A ±6 ms- Accuracy, 0.68 mm2 and 2.21 μW QRS detection ASIC',VLSI Design, vol. 2012, pp. 1-13

[18]. N. .Umapathi, G.L. 2020. Design and Implementation of Low Power 16x16 Multiplier using Dadda Algorithm and Optimized Full Adder. *International Journal of Advanced Science and Technology*. 29, 3 (Feb. 2020), 918 - 926.