An Approach to Improve the Performance of Parallel Multi-Core Processor

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Abstract- Multi-Core stands for combining the two or more processor into one integrated circuit, however in turn it provides the good performance in terms of execution while there is a tradeoff between numbers of cores, memory and power it consumes. Multicore processors give an opportunity to increase the performance of software programs by parallelizing them. However, it is not enough to have the hardware capability of parallelization through multicore. It is equally important to exploit this in software. This paper will provide the review about the evolution of multi-core processor and the difference between single core, dual core and multi-core processor along with how the performance of multi-core processor can be improved using the parallelism. Parallelization can be achieved by executing different threads of a program on multiple cores.

Index Terms: *Multiprocessors, Multi-core, Parallel Programming, Dual Core, Quad Core.*

I. INTRODUCTION

Parallel computing is Multicore of the constructs consisting of two or more separate blocks (cores) that read and write processor instructions on a single chip. A multi-core processor can execute several instructions simultaneously, which increases the speed and productivity of program execution. The original processor has one core, the dual-core processor has two cores, the quad-core processor has four cores, the six-core processor has six, eight core processors eight, deca has ten cores and so on. Gordon Moore predicted that many cores in the chip would double every 18 months, as provided cost and performance, called as Law of Moore. Not every multi-core processor must be faster than a single-core, but the overall performance of a multi-core processor is better when solving several tasks in parallel.[1]

Multi-core implementation may be different, homogenous or multisensory, as per the requirement of application. In a homogeneous architecture, all cores are identical and break the standard calculations and simultaneously work to improve the overall CPU performance. Heterogeneous kernels have more than one type of kernel, they are not identical, each core can process different applications. The latter has better performance in terms of lower power consumption, as shown later. In general, productivity refers to the time it takes to perform a particular task, which can be expressed as a frequency multiplied by the number of hours made on the clock, as stated in the formula.[2]

Performance of the System = Executed Instructions/Clock Cycle X Frequency

Full speed and operation of all cycles are essential for CPU usage, which can be increased by increasing the usage of these two features. Unfortunately, it often has a significant impact on energy use. The issue is very important, although the ITRS Roadmap is still in demand and will make 300 X or more models by 2023 with transparency and 100 X or more number of cores than usual.

Power of the System = Voltage X Voltage X Frequency

So there is a tradeoff between power and instructions per cycle to obtain either power efficiency of processor or high performance [3]

II. HISTORY OF MULTI-CORE PROCESSORS

An entire market microprocessor is designed with efficiency and cost keeping in the mind. Intel founder Gordon Moore estimates that in the semiconductor industry, the number of transistors in the chip doubles every 18 months to achieve this requirement, known as Law of Moore. Integrated power generation technology and advanced chip manufacturing technology provide integrated density, combining one billion transformers on single chip for performance improvement.

So capacity increased by regiment-dominated microarchitecture is consistent with the square root of increasing complexity. This means that the logic at the core of the processor increases performance by only 40%. Another major obstacle in modern chip technology is power consumption. Studies show that the smaller the chip capacity, the higher the transistor current, which can lead to higher power consumption.[4]

An alternative way to improve performance is to increase operating frequency, which allows programs to run faster. while frequency is currently limited to 4 GHz again, so any hike in the frequency will again increase the power distribution. "Due to the battery life and system costs, the design team will consider performance over performance in such a situation." Consumption of Power become so high that method of conventional cooling for boxes of microprocessor can be budgeted for cooling type liquid or hardware of cooling type. Eventually designers may hit the so-called power wall, which limits the amount of energy a microprocessor can waste.[5]

III. CHALLENGES IN MULTI-CORE PROCESSORS:

Despite the many benefits of multi-core infrastructure, there are several major challenges facing technology. One of the most important things about software is that it works slower on multi-core than single-core. It may be noted that "applications in multi-core systems do not automatically accelerate as the cores grow." Developers are required to write programs that use multiple operations in a multi-core environment without spending the time they need to develop programs.

Many applications are used today that operate on the same operating system and have unlimited use of multi-core processors. While software developers can develop software that can fully utilize multi-core models, the biggest challenge for the industry is how to bring back software development years ago to multi-core applications. know program. While it may seem that programs can be written, it is not a technology decision in these environments. It is a better business model when companies have to decide whether to redesign programmers, noting such factors as satisfaction of customer, Reduction in cost and market time.[6]

The business addresses the issue as designing applications that deliver software from the heart to "multi-core known" systems that can accelerate the power of multi-core vendors. Designers

can perform a "reset design" process, in which prompts execute rules, moving commands to control whether they can be executed in the same order close to each. It allows us to run modules and improve performance at the same time. Colleges will also be created to create topics or activities for a particular organization that will facilitate these activities. Intel has released important information about C ++ and Fortran devices designed for end users on multi-core processors.

Also included is Open MP (Open Multiprocessing), an application-based programming application that supports multiple programs in C language, C ++ language , and Fortran language and facilitates standards for proficient multilayer code. However, it has been widely reported that "processor bandwidth is highly efficient, energy efficient, and many answers are obtained when programming code is ready for multiple cores." Second, volcanic coupling becomes a critical issue in the design of multicore operations.

The high number of cores results in a large amount of delay (wire loss) when the data and the multicore signal can be transferred from memory.

Memory and memory management are some of the old ways to try to solve this problem. Virtual networks (IP addresses) are IP addresses (artificial intelligence) that execute and execute packets that can more efficiently transmit data to the SoC and provide less data entry. The main purpose of this chapter arises from the influence they have on the race of heads in the mainstream. "Too much at a time to access other data can lead to errors over time." the data sources before and after this initial update are memory files, and the key is in the wrong direction.

The race condition is severe and the code cannot detect it because it is done randomly. To avoid a competitive situation, you should install a special scanner with one exception. Another important aspect that affects the subsequent implementation is the relationship between it and vice versa. Shopping centers and more. Company and memory, where the main issue is car disputes and departure time. Many cloud and hardware systems have been developed to address this issue. [7]

IV. VARIOUS TYPE OF MULTI-CORE PROCESSORS

- **TILEPRO64-** This multi-core processors machine has 64 homogeneous cores that are arranged in a mesh network. Each core consists of a full-featured processor, L1 and L2 cache, and a non-blocking switch that connect the core with the whole mesh. The Tile pro family incorporates Tilera's Dynamic Distributed Cache (DDC) technology which accelerates the cache coherence performance by a factor of two when compared to other multi-core processors machines.

The TIELPro64 has many attractive features such as the massively scalable performance, power efficiency, and it is considered as an Integrated solution. Its processor cores combines the features of a general-purpose Central Processing Unit (CPU) along with a powerful signal processing and Single Instruction, Multiple Data (SIMD) capabilities, which will result in

integrating multiple functionalities on the same single processor that reduces the system cost and simplifies the system design.

It uses a 32-bit Very Long Instruction Word (VLIW) processors with 64-bit instruction bundle, and its pipeline has a 3-deep pipeline with up to 3 instructions per cycle resulting in executing 12 times the instructions if compared to a single-core. Its on-chip cache size 5.6 Mbytes, executes up to 443 billion operations per second (BOPS), and 200 Gbps memory bandwidth with four 64-bit DDR2 controllers [6]. If VLIW is combined with the MIMD (multiple instruction, multiple data) processors, multiple operating systems could be run in a simultaneous order and advanced multimedia applications such as video conferencing and video-on-demand could be run more efficiently [3].

- **EPIPHANY-IV 64-CORE 28NM MICROPROCESSOR (E64G401)**

This multi-core processors machine has 64 High Performance Reduced Instruction Set Computer (RISC) CPU Cores arranged in a 8 * 8 mesh network, each core operates at 800 MHz and 1.6 GFLOPS/sec. The CPU has an efficient general-purpose instruction set that excels at compute intensive applications while being efficiently programmable in C/C++ without any need to write code using assembly or processor specific intrinsics [8].

This machine's memory architecture is based on a flat memory map in which each compute node has a small amount of local memory as a unique addressable slice of the total 32-bit address space.

A processor can access its own local memory and other processors memory through regular load/store instructions, with the only difference being the latency and effective throughput of the transactions. The local memory system is comprised of 4 separate banks, allowing for simultaneous memory access by the instruction fetch engine, local load-store instructions, and by load/store transactions initiated by other processors within system [8].

V. ANALYSIS OF PROCESSOR'S PERFORMANCE

Many tools can be used to measure system performance, such as: throughput, which is the degree of process kill success; response time, which is the time between the request time and the operating system starting to work on the request;

Runtime, which is the time needed to fulfill the request, its capacity, as well as memory bandwidth, which is a constant amount of data between the master and RAM. All of these systems can be divided into three main categories: higher quality, better lower quality, and higher quality. For example, higher performance is better, less execution time better, and better quality control [5]-[17].

VI. MULTI CORE ARCHITECHURE

Muti-Core processor could be understood with the help of using single core multiple time so here there is typical architecture define below for single core computer. However the architecture is very basic but needs to be described for better understanding.

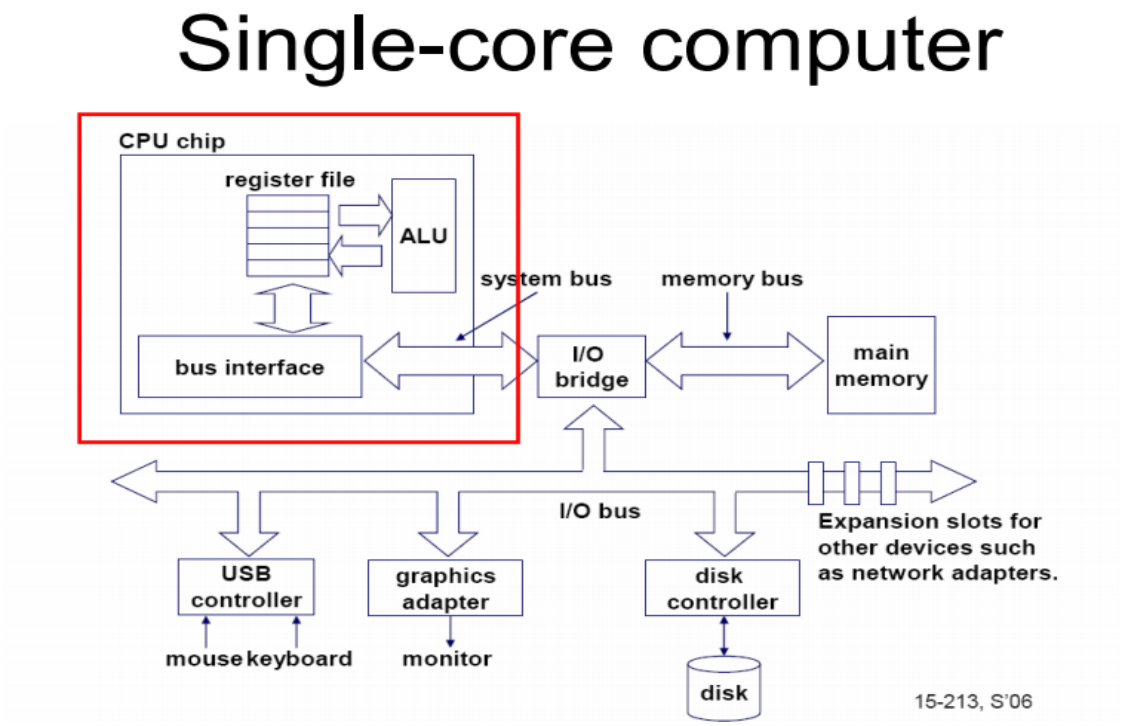


Fig-1: Archieture of Single Core Computer

In above figure -1 architecture of Single Core Computer everything is explained in a very basic way that how and what CPU chip contains & communicate with other resources like I/O , Main Memory, USB's and other peripherals.

Here in below figure -2, we have defined the typical architecture of single core CPU functionality however it is very basic but it is required to understand the functionality of entire system that is multi core systems.

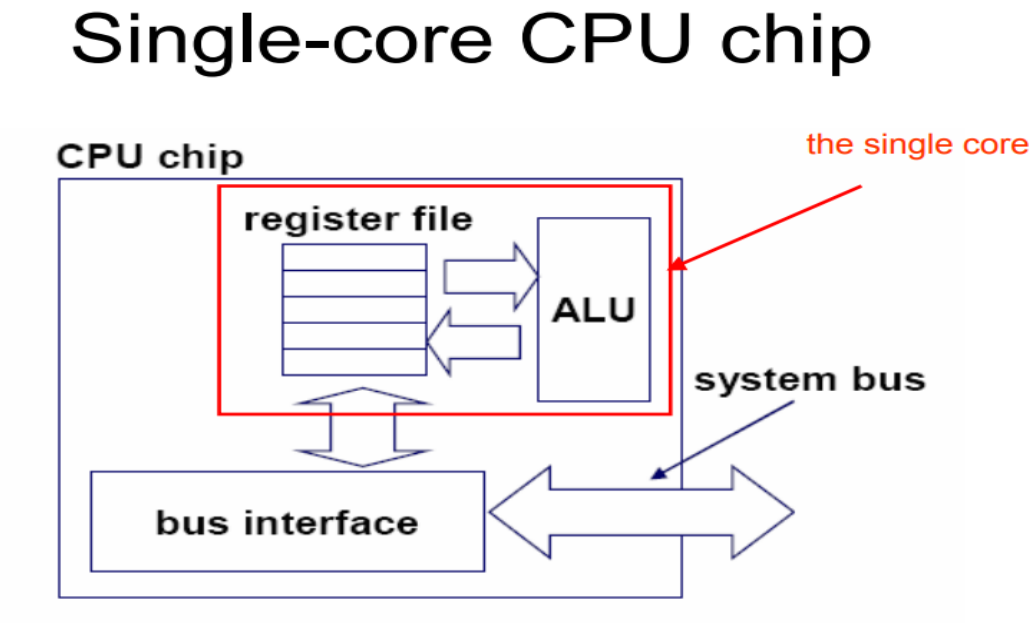


Fig-2: Archieture of Single Core CPU

Here in below figure -3, we have defined the typical architecture of multi core CPU functionality. Here is an example of combination of four cores. It is explained in below figure about the functionality of quad core processor. Each register file will be processed by corresponding ALU. Entire architecture system i.e quad core will be using same bus interface.

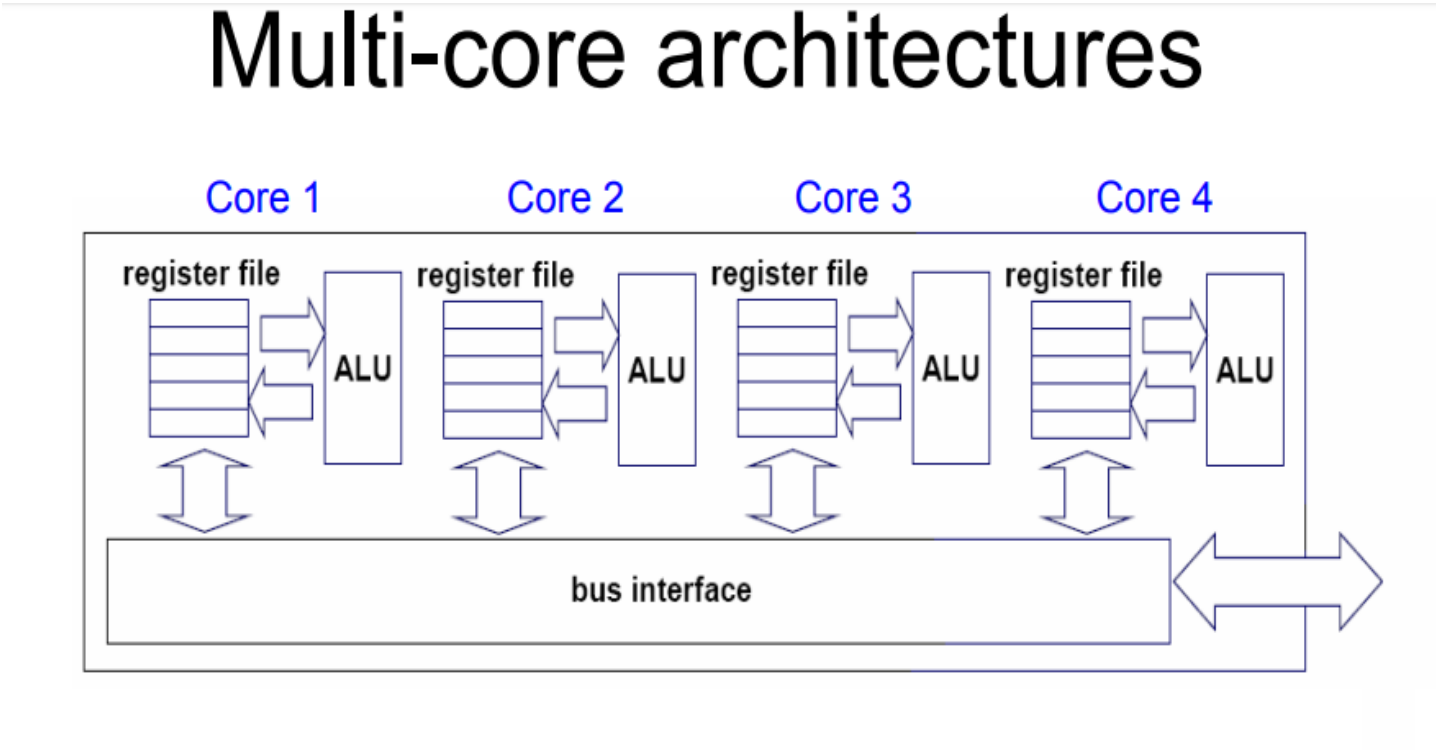


Fig-3: Architecture of Multi- Core CPU

Here in below figure4 the processing of muti core CPU chip is defined below.

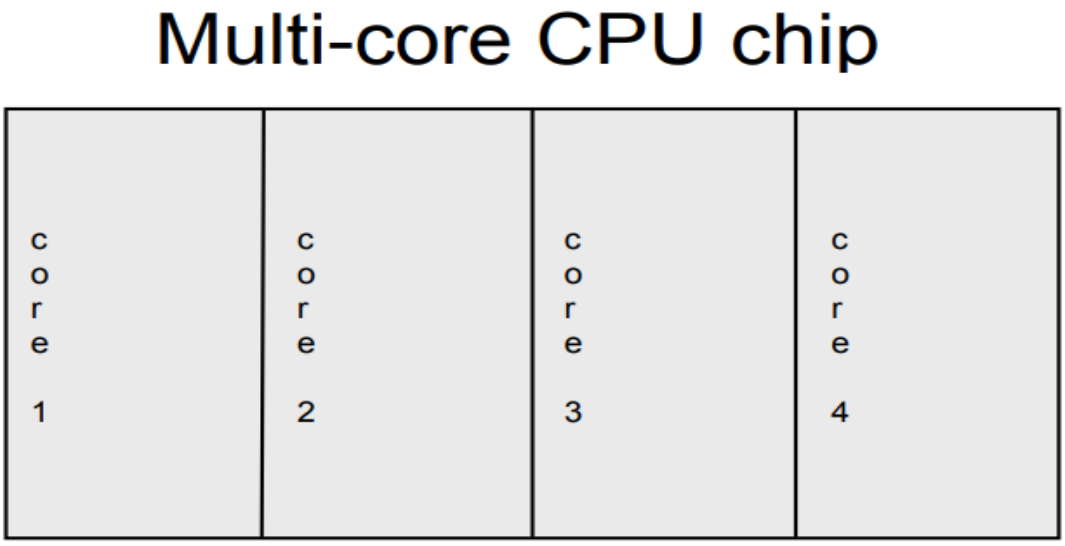


Fig-4: Processing of Multi- Core CPU

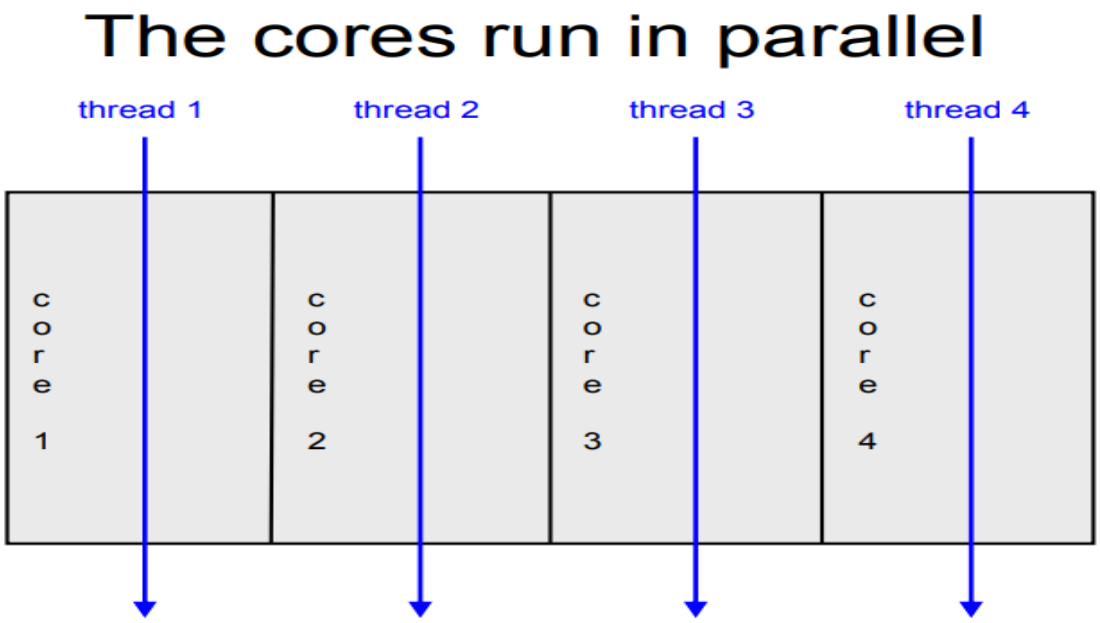


Fig-5: Processing of Multi- Core CPU in parallel

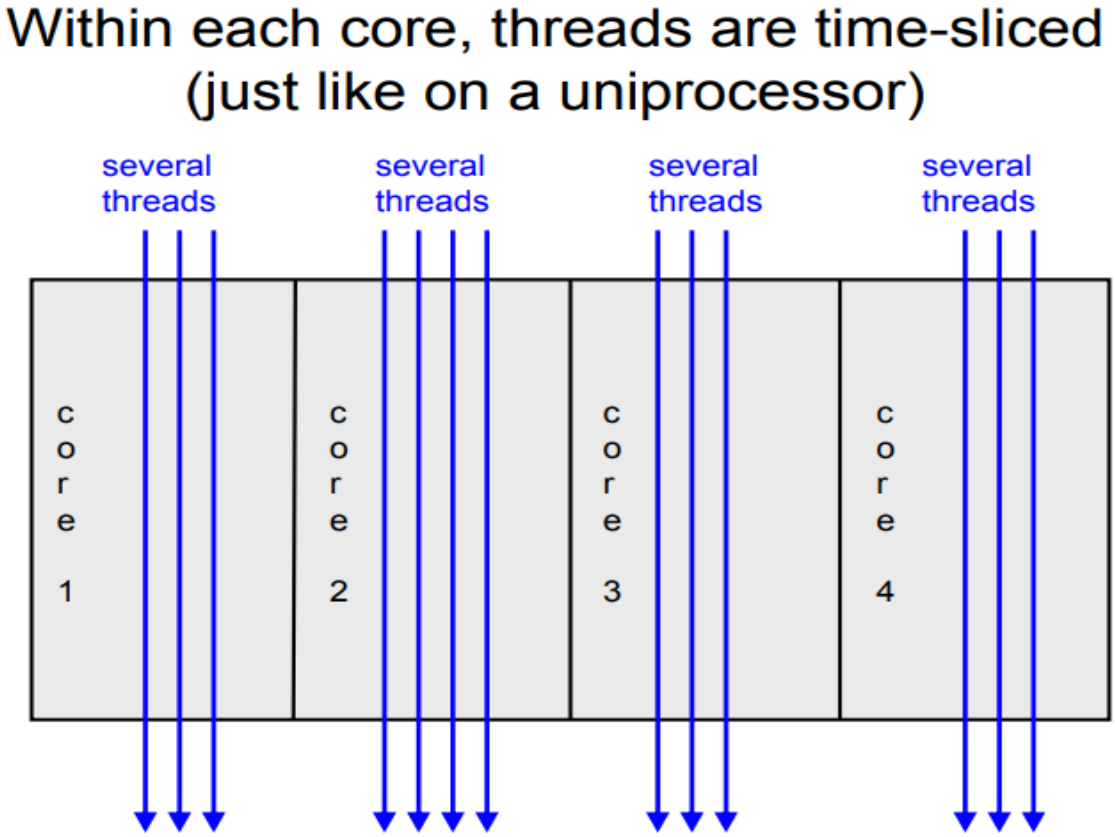
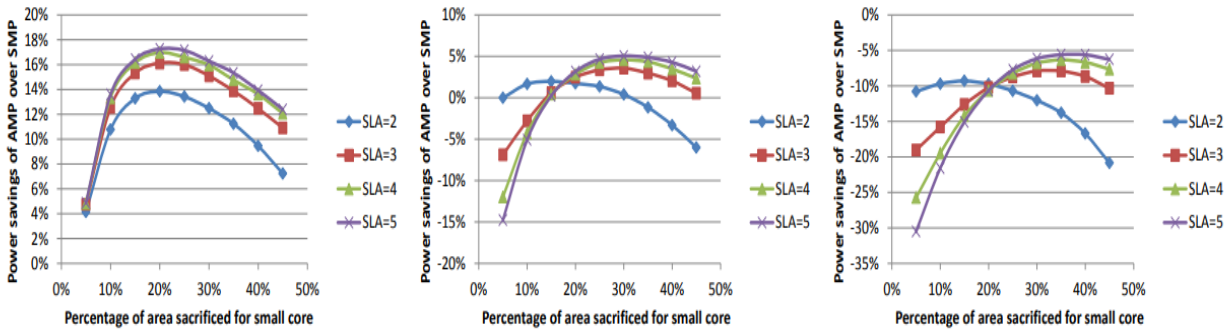


Fig-6: Processing of Multi- Core CPU in parallel

VII. RESULT ANALYSIS

As far as result analysis is concern here Power impact of using asymmetric multicore processors (AMP) configurations for energy scaling is defined for various cores like small cores bais, uniform core bias and Large core bias that is in comparison to power comparison.



(a) Small core bias. (b) Uniform bias. (c) Large core bias.

Power impact of using asymmetric multicore processors (AMP) configurations for energy scaling

VIII. CONCLUSION

The release of the first dual-core processor we enter a new era in processor architecture. Dual-core and multi-core processors become the standard for delivering greater performance, improved performance per watt, and new capabilities across desktop, mobile, and server platforms. Platforms built around the dual-core processors are ideal for enthusiasts who crave computing power for audio, video, digital design and gaming applications from one side and multitasking scenarios in business from latter one. Multi-core capabilities can enhance user experiences in multitasking environments, namely, where a number of foreground applications run concurrently with a number of background applications such as virus protection and security, wireless, management, compression, encryption and synchronization. Multi-core chips do more work per clock cycle, and can be designed to operate at the lower frequencies than their single-core counterparts. All of this makes significantly improved user experiences in both home and business environments and the same time extends Moore's Law well into the future With the launch of the first dual-core processor, we are entering a new era of architecture. Media interfaces are the standard for improving the performance, wadding efficiency, and new features of desktop, mobile, and service platforms. Developed in the presence of mobile applications, the platform is ideal for enthusiasts who want to collaborate on content, video, digital images and video game products and engage in a growing product market. Three. Many features can enhance the user experience in a versatile environment, and many applications use a variety of backups, such as antivirus, security, wireless, control, compression, encryption, and synchronization. My multi-core chip works for over an hour and may run slower than others. All of these factors will improve the user experience both at home and in the business, extending Moore's Law in the future.[18]-[20]

IX. REFERENCES

[1] "Concurrency is not Parallelism", Waza conference Jan 11, 2012, Rob Pike (slides) (video).

[2] Flynn, Laurie J. (8 May 2004). "Intel Halts Development of 2 New Microprocessors ". New York Times. Retrieved 5 June 2012.

[3] B. Schauer, "Multicore processors – a necessity." ProQuest discovery guides (2008): 1-14.

[4] Krauss, Kirk J (2018). "Thread Safety for Performance". Develop for Performance. Retrieved 2018-05-10.

[5] D. Ismail, “Multi-Core Processor Performance Analysis – A Survay,” [Online]. Available: http://www.cse.wustl.edu/~jain/cse567-13/ftp/multicore/index.html

[6]Tilera Corporation, “Tilepro64 Processor,” [Online]. Available: http://www.tilera.com/sites/default/files/productbriefs/TILEPro64_Processor_PB019_v4.pdf

[7] Blake, G., Dreslinski, R.G. & Mudge, T. 2009, "A survey of multicore processors ", Signal Processing Magazine, IEEE, vol. 26, no. 6, pp. 26-37.

[8] adapteva, "Epiphany-IV 64-core 28nm Microprocessor (E64G401),” [Online]. Available: http://www.adapteva.com/products/silicon-devices/e64g401/

[9] IRakhee Chhibber, IIDr. R.B.Garg, Multicore Processor, Parallelism and Their Performance Analysis, International Journal of Advanced Research in Computer Science & Technology (IJARCST 2014).

[10] M.Khanafseh, O.Surakhi & Y.Jaffal,“Parallel Implementation of "Fast algorithm for Project Clustering" on Multi Core Processor using Multi Threads”, Journal of Computer Science IJCSIS June 2017 Part I.pdf, (pp. 248-255)

[11] Heba Mohammed Fadhil, Mohammed Issam Younis, “Parallelizing RSA Algorithm on Multicore CPU and GPU”, International Journal of Computer Applications (0975 – 8887) Volume 87 – No.6, February 2014

[12] Badr Benmammar, Youcef Benmouna, Asma Amraoui, Francine Krief,” A Parallel implementation on a Multi-Core Architecture of a Dynamic Programming Algorithm applied in Cognitive Radio Ad hoc Networks”, International Journal of Communication Networks and Information Security (IJCNIS), Vol. 9, No. 2, August 2017

[13] Subhi A. Bahudaila and Adel Sallam M. Haider, “Performance Estimation of Parallel Face Detection Algorithm on Multi-Core Platforms”, Egyptian Computer Science Journal Vol. 40 No.2 May 2016, ISSN-1110-2586

[14] Sheela Kathavate, N.K. Srinath, “Efficiency of Parallel Algorithms on Multi Core Systems Using OpenMP”, International Journal of Advanced Research in Computer and Communication Engineering Vol. 3, Issue 10, October 2014

[15] Muti-Core Processors—The Next Evolution in Computing http://multicore.amd.com/Resources/33211A_Multi-Core_WP_en.pdfvisited on 16/09/2017

[16]Karthik Lakshmanan, Shinpei Kato, Ragunathan (Raj) Rajkumar “Scheduling Parallel Real-Time Tasks on Multi-core Processors”, Dec 2010, Page(s):259-268.

[17] Constantinos Christofi, George Michael, Pedro Trancoso and Paraskevas Evripidou “Exploring HPC Parallelism with Data-Driven Multithreading”, Sept 2012, Page(s):10-17.

[18] Sodan, A., Machina, J., Deshmeh, A., Macnaughton, K. & Esbaugh, B. 2010, "Parallelism via Multithreaded and Multicore CPUs", Computer, vol. PP, no. 99, pp. 1-1.

[19] Thomas Rauber; Gudula Rünger (2013). Parallel Programming: for Multicore and Cluster Systems. Springer Science & Business Media. p. 2. ISBN 9783642378010.

[20] Geoffrey Blake, Ronald G. Dreslinski, and Trevor Mudge, “A Survey of Multicore Processors “, IEEE SIGNAL PROCESSING MAGAZINE NOVEMBER 2009

[21]ZODPE, HARSHALI, et al. "SCALABLE ARCHITECTURE FOR COMPUTATIONALLY INTENSIVE APPLICATIONS. International Journal of Electronics and Communication Engineering (IJECE) ISSN 2278-9901 Vol. 2, Issue 4, Sep 2013, 33-40

[22] Chowdary, Undavalli Vivek, et al. "Home automation system using IR sensors." *International Journal of Electrical and Electronics Engineering (IJEEE)* 4.6 (2015): 11-16.